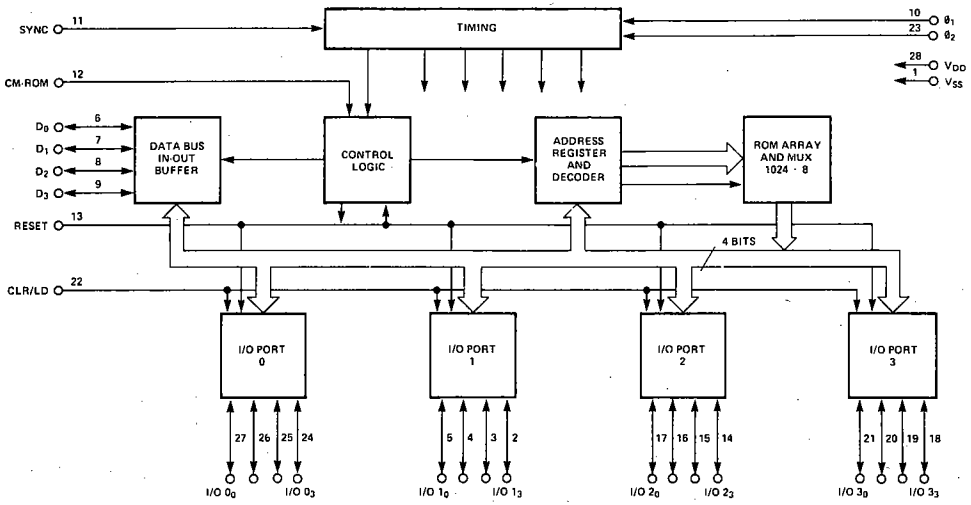
4308
1024 x 8 MASK PROGRAMMABLE ROM AND FOUR 4-BIT I/O PORTS

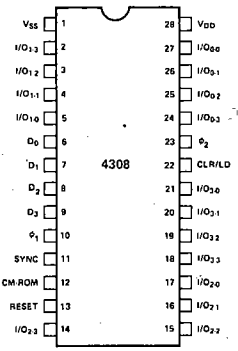
- **Direct Interface to MCS-40™ 4-Bit Data Bus**
- **Equivalent to Four 4001 ROMs**
- **Four Independent 4-Bit I/O Ports**
- **Input I/O Buffer Storage with an Optional Strobe**
- **I/O Ports Low-Power TTL Compatible**
- **28 Pin Dual In-Line Package**
- **Standard Operating Temperature Range of 0° to 70° C**
- **Also Available With -40° to +85° C Operating Range**

The 4308 is a 1024 x 8 bit word ROM memory with four I/O ports. It is designed for the MCS-40™ system and is operationally compatible with all existing MCS-40 elements. The 4308 is functionally identical to four 4001 chips. The 4308 has 16 I/O lines arranged in four groups of four lines.

BLOCK DIAGRAM



PIN CONFIGURATION



Pin Description

Pin No.	Designation/ Type of Logic	Description of Function
1	V_{SS}	Most positive supply voltage.
2-5 14-17 18-21 24-27	$I/O1_3$-$I/O1_0$/Neg. $I/O2_3$-$I/O2_0$/Neg. $I/O3_3$-$I/O3_0$/Neg. $I/O0_3$-$I/O0_0$/Neg.	Four I/O ports consisting of 4 bidirectional and selectable lines.
6-9	D_0-D_3/Neg.	Bi-directional data bus. All information between processor and device is transmitted to these four pins.
10, 23	$\phi1$, $\phi2$/Neg.	Non-overlapped clock signals which determine device timing.
11	SYNC/Neg.	System synchronization signal generated by processor.
12	CM-ROM/Neg.	Chip enable generated by the processor.
13	RESET/Neg.	Reset input. A negative level (V_{DD}) on this pin will clear internal flip-flops and buffers. The input buffers are not cleared by this signal.
22	CLR/LD/Neg.	Clear/Load input. This pin is a dual function pin. It may be selected as a common Clear for those pins selected as output pins or as a Load for those pins selected as input pins. This pin should be designated for one purpose only per 4308, either Clear or Load. As a Load, a positive (V_{SS}) to negative (V_{DD}) transition will cause the I/O data to be placed in the input latch. A negative to positive transition will cause the data to be latched. The I/O pin state may be altered without changing the contents of the latch when the line is positive. As a Clear, a negative level (V_{DD}) on this line will cause the designated output latches to clear and remain cleared until a positive level (V_{SS}) is placed on the line. This line may be driven by a TTL output with a 1K pull-up resistor to V_{SS}.
28	V_{DD}	Main supply voltage. Value must be V_{SS} -15V ±5%.

Functional Description

The 4308 ROM program memory is arrayed 1024 x 8 bit words. For the program memory mode of operation, the A1 –A3 time periods of the instruction cycle are used to address the ROM contents. The 4308 decodes the first ten bits of the address to select 1 out of the 1024 words, 8 bits wide. The remaining two bits select a particular 4308, which has one of four possible metal option chip select addresses. Instruction information is available in two 4-bit segments during M_1 and M_2 time periods. A 4004 system can accommodate up to four 4308's while a 4040 system can utilize up to eight devices.

A second mode of operation of the ROM is as an Input/Output control device. In that mode a ROM chip will route information to and from data bus lines in and out of 4 I/O external lines. Each chip has the capability to identify itself for an I/O port operation, recognize an I/O port instruction and decide whether it is an Input or an Output operation and execute the instruction.

All internal flip flops (including the output register) will be reset when the RESET line goes low (negative voltage).

Each of the four I/O ports of a 4308 are program selectable. Each of the four lines can be specified as either inputs or outputs via a metal mask option. A complete description of the I/O option capabilities are given below. The 4308 has an input storage buffer for utilization with those I/O pins designated as inputs. A common strobe line (CLR/LD line) allows the loading of data from the I/O lines. The same CLR/LD strobe line can also serve as a clear to the I/O output port buffers when designated. This CLR/LD line is common to all ports on a 4308 and when toggled, will effect those I/O lines connected by the metal mask option. For an input line, if the CLR/LD strobe line is left unconnected, of if it is pulled to (V_{DD}), then the output fo the buffer will follow the input.

NOTE: Since the 4308 is compatible with all components of the MCS-40 system, 4308 and 4001 can be mixed on one memory bank as long as the chip select addresses are mutually exclusive.

The following table shows the chip number relationship between 4308 and 4001.

4308		4001	
Page No.	Chip No.	Page No.	Chip No.
0-3	(0)	0-15	0-15
4-7	(1)		
8-11	(2)		
12-15	(3)		

INSTRUCTION EXECUTION

The 4308 responds to the following instructions.

1. **SRC Instruction** (Send address to ROM and RAM)

   When the CPU executes an SRC instruction it will send out 8 bits of data during X_2 and X_3 and will activate the CM-ROM and one CM-RAM line at X_2. Data at X_2 (representing the contents of the first register of the register pair addressed by the SRC instruction), with simultaneous presence of CM-ROM, is interpreted by the 4308 as the chip number of the unit that should later perform an I/O operation. Data at X_3 is ignored. After an SRC only one CM-ROM and CM-RAM device will be selected.

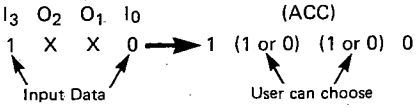
2. **WRR – Write ROM Port**

   The content of the accumulator is transferred to the ROM output port of the previously selected ROM chip. The data is available on the output pins until a new WRR is executed to the same port. The ACC content and carry/link are unaffected. The LSB bit of the accumulator appears on I/O_0.) No operation is performed on I/O lines coded as inputs.

3. **RDR – Read ROM Port**

   The data present at the input lines of the previously selected ROM chip is transferred to the accumulator.

   If the I/O option has both inputs and outputs within the same 4 I/O lines, the user can choose to have either "0" or "1" transferred to the accumulator for those I/O pins coded as outputs, when an RDR instruction is executed. For example, given a port with the I/O lines coded with 2 inputs and 2 outputs, when RDR is executed the transfer is as shown below:



Timing Considerations

At the beginning of each instruction sequence, a SYNC pulse is generated externally to synchronize the processor with the various components of the system. This pulse, along with the clock inputs ϕ_1 and ϕ_2, is used in the 4308 as an input to a timing register.

During time A_1, A_2, and A_3, the address is sequentially accepted from the data bus and decoded. During time A_3, the CM-ROM line will be active, and if the 2 highest order bits of the address sent at A_3 match the metal preprogrammed chip select option, the ROM will respond to the current address.

At time M_1 and M_2, the instruction OPR, OPA will be placed on the data bus for the processor.

After the SRC or Send Register Control instruction, which is used to designate a set of 4 I/O lines (1 port) on a particular ROM which are to be used for subsequent ROM I/O operations, is executed by the processor, the processor sends a 4 bit code to the ROM during X_2, and CM-ROM goes to a "1" (V_{DD}). The first two bits (D_3, D_2) of this code select a group of 1 out of 4 possible 4308, and the last two bits select a particular port (1 of 4 ports). This port remains selected until the next SRC instruction is executed.

In both the RDR and WRR operations, the CM-ROM line will become active during time M_2, and if the ROM has a previously selected I/O port, it will respond to the I/O in two ways. For a WRR accumulator, data will be transferred to an internal ROM selected output port flip-flops during X_2. Data will be available on the I/O line from time $X_3 \cdot \overline{\phi_2}$. The data will remain on the bus until a new WRR occurs, a reset occurs, or a clear (CLR/LD line) is generated. The RDR instruction will transfer information from the input port flip-flops of a previously selected port. Prior to RDR instruction, the user should insure that the input flip-flops have been loaded via the CLR/LD strobe if the load strobe is specified. If the load strobe is not specified, information on the input lines will be loaded into the accumulator at the time of the RDR.

I/O OPTIONS

The 4308 offers the following options on its I/O pins:

1. Input or output.
2. Inverted or direct (for input and output).
3. On-chip resistor connected to either V_{SS} or V_{DD} for input pins.
4. Loading of input buffers via the CLR/LD signal.
5. Clear signal for any or all output ports via the CLR/LD signal.

Referring to the block diagram of the single I/O pin shown below which illustrates the various options available on a 4308, it should be noted that certain pin combinations are mutually exclusive and should not be specified together. There are also certain invalid combinations. The following combinations should be avoided:

8,9
5,6
3,4
10,11 — Both on a single pin and within a single 4308.

Examples of some common desired option/connections are:

a. *I/O pin inputs**

non-inverting	11, 2, 5, 7, 9 (TTL) – 2, 5, 7, 8
inverting	11, 2, 6, 7, 9 (TTL) – 2, 6, 7, 8

b. *I/O pin outputs*

non-inverting	3, 1 (10 optional)
inverting	4, 1 (10 optional)

Other combinations exist and should be used with caution.

**Option 11 need not be specified if an unbuffered input is desired. This is equivalent to a 4001 input.*

NOTE: The 4308 has the following enhancements over the 4001 as far as I/O options are concerned:

1. The capability of clearing any or all outputs with the CLR/LD signal.
2. TTL compatibility of both the inverting and non-inverting input paths for input ports.
3. The capability to select the LD option and have the input buffer become an input flip-flop and to have the CLR/LD signal become a clock for loading data.

For TTL compatibility on the I/O lines, the supply voltage should be V_{DD} = -10V ±5%, V_{SS} = +5V ±5%. External pull-up is required for outputs.

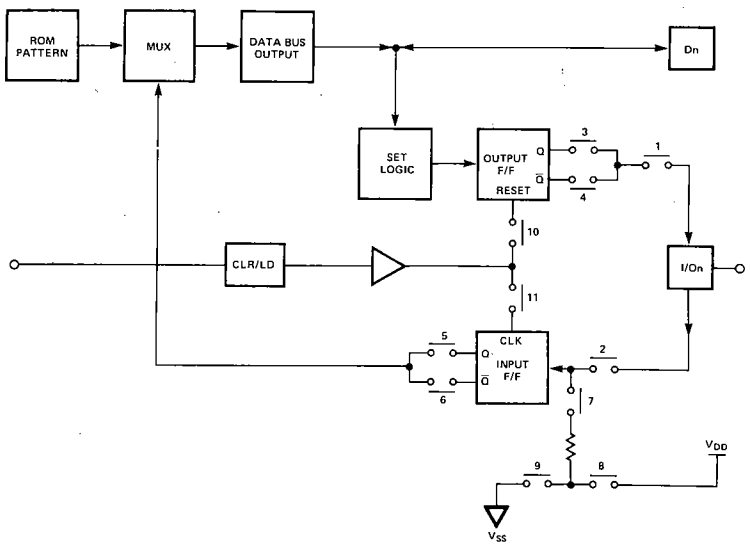


Figure 1. 4308 I/O Pin Options.

Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... -55°C to + 125°C
Input Voltages and Supply Voltage
with respect to Vss ..... +0.5V to -20V
Power Dissipation ..... 1.0 Watt

*COMMENT:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

D.C. and Operating Characteristics

T_A = 0°C to 70°C; V_{SS} -V_{DD} = 15V ±5%; $t_{\phi PW}$ = $t_{\phi D1}$ = 400 nsec; $t_{\phi D2}$ = 150 nsec; Logic "0" is defined as the more positive voltage (V_{IH}, V_{OH}); Logic "1" is defined as the more negative voltage (V_{IL}, V_{OL}); Unless Otherwise Specified.

SUPPLY CURRENT

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
I_{DD}	Average Supply Current		20	40	mA	T_A = 25°C
INPUT CHARACTERISTICS – ALL INPUTS EXCEPT I/O PINS						
I_{LI}	Input Leakage Current			10	μA	V_{IL} = V_{DD}
V_{IH}	Input High Voltage (Except Clocks)	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage (Except Clocks)	V_{DD}		V_{SS}-5.5	V	
V_{ILO}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	CLR/LD pin
V_{IHC}	Input High Voltage Clocks	V_{SS}-1.5		V_{SS}+.3	V	
V_{ILC}	Input Low Voltage Clocks	V_{DD}		V_{SS}-13.4	V	
OUTPUT CHARACTERISTICS – ALL OUTPUTS EXCEPT I/O PINS						
I_{LO}	Data Bus Output Leakage Current			10	μA	V_{OUT} = -12V
V_{OH}	Output High Voltage	V_{SS}-.5V	V_{SS}		V	Capacitive Load
I_{OL}	Data Lines Sinking Current	8	15		mA	V_{OUT} = V_{SS}
V_{OL}	Output Low Voltage, Data Bus, CM, SYNC	V_{SS}-12		V_{SS}-6.5	V	I_{OL} = 0.5mA
R_{OH}	Output Resistance, Data Line "0" Level		200	300	Ω	V_{OUT} = V_{SS} -.5V
I/O INPUT CHARACTERISTICS						
I_{LI}	Input Leakage Current			10	μA	
V_{IH}	Input High Voltage	V_{SS}-1.5		V_{SS}+.3	V	
V_{IL}	Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
V_{IL}	CLR/LD Input Low Voltage	V_{DD}		V_{SS}-4.2	V	
R_I	Input Resistance, if Used	10	18	35	kΩ	R_I tied to V_{SS}; V_{IN} = V_{SS} -3V
R_I[1]	Input Resistance, if Used	15	25	40	kΩ	R_I tied to V_{DD}; V_{IN} = V_{SS} -3V
I/O OUTPUT CHARACTERISTICS						
V_{OH}	Output High Voltage	V_{SS}-.5V			V	I_{OUT} = 0
R_{OH}	I/O Output "0" Resistance		1.2	2	kΩ	V_{OUT} = V_{SS} -.5V
I_{OL}	I/O Output "1" Sink Current	2.5	5		mA	V_{OUT} = V_{SS} -.5V
I_{OL}[2]	I/O Output "1" Sink Current	0.8	3		mA	V_{OUT} = V_{SS} -4.85V
I_{CF}	I/O Output "1" Clamp Current			4	mA	V_{OUT} = V_{SS} -6V; T_A = 70°C
V_{OL}	I/O Output Low Voltage	V_{SS}-12		V_{SS}-6.5	V	I_{OUT} = 50μA

Notes: 1. R_I is large signal equivalent resistance to (V_{SS} -12) V.
2. For TTL compatability, use 12kΩ external resistor to V_{DD}.

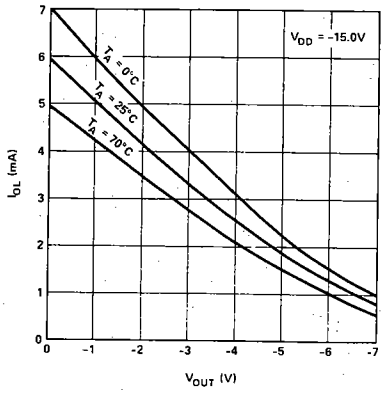
MCS 4/40

D.C. and Operating Characteristics

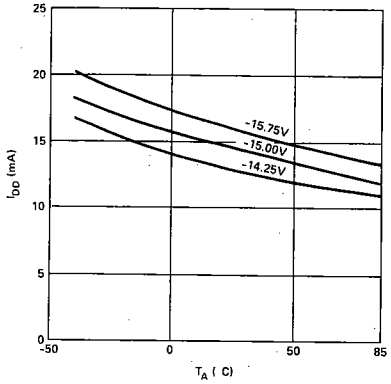
CAPACITANCE

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
C_ϕ	Clock Capacitance		14	20	pF	$V_{IN} = V_{SS}$
C_{DB}	Data Bus Capacitance		7	10	pF	$V_{IN} = V_{SS}$
C_{IN}	Input Capacitance			10	pF	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance			10	pF	$V_{IN} = V_{SS}$

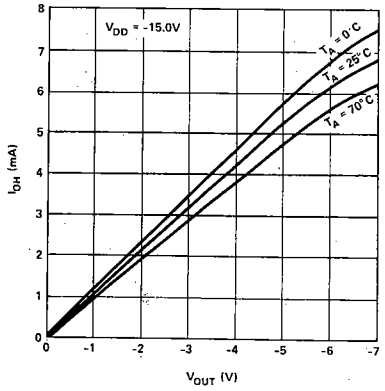
4308 OUTPUT PINS ("1" LEVEL)



4308 SUPPLY CURRENT VS. TEMPERATURE



4308 OUTPUT PINS ("0" LEVEL)



A.C. Characteristics

T_A = 0°C to 70°C, V_{SS} -V_{DD} = 15V ±5%

Symbol	Parameter	Limit Min.	Typ.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	1.35		2.0	μsec	
$t\phi_R$	Clock Rise Time			50	ns	
$t\phi_F$	Clock Fall Time			50	ns	
$t\phi_{PW}$	Clock Width	380		480	ns	
$t\phi_{D1}$	Clock Delay ϕ_1 to ϕ_2	400		550	ns	
$t\phi_{D2}$	Clock Delay ϕ_2 to ϕ_1	150			ns	
t_W	Data-In, CM, SYNC Write Time	350	100		ns	
t_H[1,3]	Data-In, CM, SYNC Hold Time	40	20		ns	
t_{OS}[2]	Set Time (Reference)	0			ns	
t_{ACC}	Data-Out Access Time					C_{OUT} =
	Data Lines			930	ns	500pF Data Lines[4]
	SYNC			930	ns	500pF SYNC
	CM-ROM			930	ns	160pF CM-ROM
	CM-RAM			930	ns	50pF CM-RAM
t_{OH}	Data-Out Hold Time	50	150		ns	C_{OUT} = 20pF
t_{IS}	I/O Input Set-Time	50			ns	
t_{IH}	I/O Input Hold-Time	100			ns	
$t_{PW\ I/O}$	C/L Pulse-Width	1000	400		ns	
$t_{W\ C/L}$	C/L Write Time	350	200		ns	
$t_{H\ C/L}$	C/L Hold Time	100			ns	
t_D	I/O Output Delay			1500	ns	C_{OUT} = 100pF
t_C[5]	I/O Output Delay on C/L		750	1500	ns	C_{OUT} = 100pF
$t_{W\ \phi 2F}$[6]	Data In Write Time with Respect to ϕ_2	-30	-60		ns	

Notes: 1. t_H measured with $t_{\phi R}$ = 10nsec.
2. T_{ACC} is Data Bus, SYNC and CM-line output access time referred to the ϕ_2 trailing edge which clocks these lines out. t_{OS} is the same output access time referred to the leading edge of the next ϕ_2 clock pulse.
3. All MCS-40 components which may transmit instruction or data to 4004/4040 at M_2 and X_2 always enter a float state until the 4004/4040 takes over the data bus at X_1 and X_3 time. Therefore the t_H requirement is always insured since each component contributes 10μA of leakage current and 10pF of capacitance which guarantees that the data bus cannot change faster than 1V/μs.
4. t_{ACC}, 4308 is guaranteed with $t_{\phi D2}$ = 200 nsec.
5. C/L Clears output buffer when low. C/L enters data into input buffer when low. C/L rising edge latches input buffer. Port Option 10 and 11 are mutually exclusive on any 4308.
6. Data Bus Inputs are guaranteed valid before ϕ_2 falling edge by 4004, 4040 t_{ACC}. If $t_{PW\phi 2}$ is widened, then t_{CY} is increased and Data Bus Inputs remain valid before ϕ_2 falling edge. Thus, $t_{W\phi 2F}$ is not a system constraint.

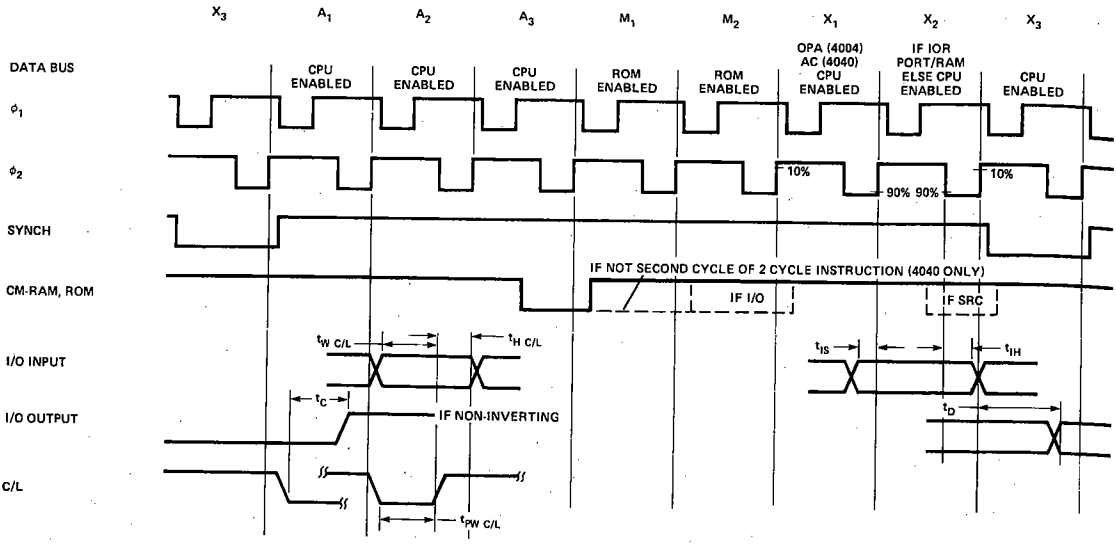


Figure 2. Timing Diagram.

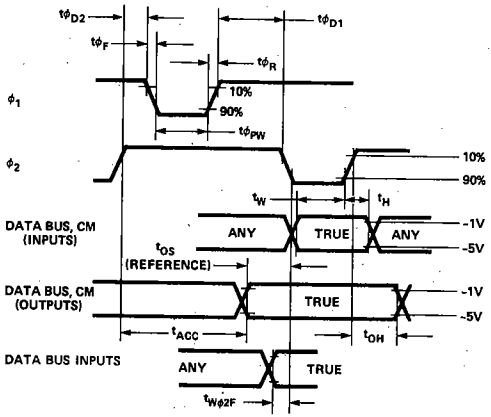


Figure 3. Timing Detail.

Programming Instruction

To insure optimum handling of ROM programs and avoid delays, programs should be specified in the following format.

Paper Tape Format*

A 1" wide paper tape using 8 bit ASCII code, such as a model 33ASR teletype produces:

A. Preamble

1. Preceding the first word field and following the last word field, there should be a leader/trailer length of at least 25 characters. This should consist of rubout punches.

2. Included in the tape before the leader, and preceded by another leader, should be the customer's complete telex or twx number and if more than one pattern is being transmitted, the ROM pattern number.

3. The first ROM pattern preamble field is the device type number or ROM number. The field should be framed by an "1" and "–"

   14308–

   This should be followed by the chip select information encoded in decimal (two digits), and enclosed by "C" and "S", as in

   "ChhS"

   The valid select digits for the 4308 are 0–3

   "C0S" – "C3S"

   Finally, the I/O options would be specified on a port-by-port basis with the connections to be made separated by commas, and enclosed in parentheses:

   "(n1, n2, n3 . . .)".

   where (n1, n2 . . .) are the option numbers associated with one I/O line. Hence, for the 4308 there will be sixteen bracketed collections of I/O options.

   Each I/O pin has a series of 11 possible connections. These connections are consecutively numbered from 1-11. It is these numbers that should be in parentheses for each I/O pin.

   Example: "( )" indicates no connection
   "(1)" indicates only #1
   "(2,5,7)" indicates connections #2, 5 and 7.

   I/O options should be placed on the tape sequentially for the 4308, from $I/O0_0$ – $I/O3_3(16)$. Always avoid illegal combinations.

NOTE: Cards may also be submitted.

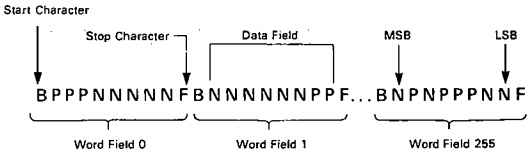
B. ROM Code

The format requirements are as follows:

1. All word fields are to be punched in consecutive order, starting with word field 0 (all addresses low). There must be exactly N word fields for the N x 8 ROM organization.

2. Each word field must begin with the start character B and end with the stop character F. There must be exactly 8 data characters between the B and F. Within the word field, a P results in a high level output (V_{SS} or logic 0 for MCS-40 CPUs) and a N results in a low level output (V_{DD} or logic 1 for MCS-40 CPUs).

   Example of 256 x 8 format (N=256):



3. Between word fields, comments not containing B's or F's may be inserted. Carriage return and line feed characters should be inserted (as a "comment") just before each word field (or at least between every four word fields). When these carriage returns, etc., are inserted, the tape may be easily listed on the teletype for purposes of error checking. It may be helpful to insert the word number (as a comment) at least every four word fields.

4. Within the ROM pattern words a character, "X", may be used. Where "P" and "N" indicate a "0" and "1" setting respectively, an "X" will indicate a single bit – "Don't Care" setting. This allows the optimum default bit values to be selected by Intel. The bit value will be fixed to allow for testing. The values will be specified to the user on the Verification Listing tape.

   In the place of a standard BPNF word, a "B*nF" word may be used. This indicates that the data in the last BPNF word encountered is to be repeated for the next n words ($1 \leq n \leq 1023$). Note that if a repeat count of 4 is given in word position 10, then words 10, 11, 12, and 13 will be repeats of word 9 (except for Don't Care bits which might conceivably have different assigned values).

   To indicate that an entire block (such as the remainder of a ROM) is not used (i.e., Don't Care), a word of Don't Care data can be followed by the remaining word count in a repeat count form.

MCS® CUSTOM ROM ORDER FORM

4308 ROM

CUSTOMER _____

P.O. NUMBER _____

DATE _____

For Intel use only

S# _____ PPPP _____

STD _____ ZZ _____

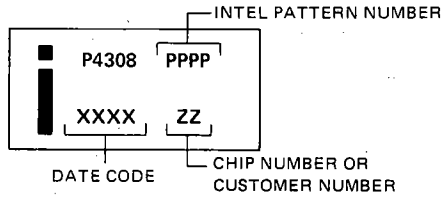
_____ DD _____

APP _____ DATE _____

All custom 4308 ROM orders must be submitted on this form. Programming information should be sent in the form of compute punched cards or punched paper tape per the formats designated on this order form. Additional forms are available from Intel

MARKING

The marking as shown at the right must contain the Intel logo, the product type (P4308), the 4-digit Intel pattern number (PPPP), a date code (XXXX), and the 2-digit chip number (DD). An optional customer identification number may be substituted for the chip number (ZZ). Optional Customer Number (maximum 6 characters or spaces).



CUSTOMER NUMBER _____

MASK OPTION SPECIFICATION

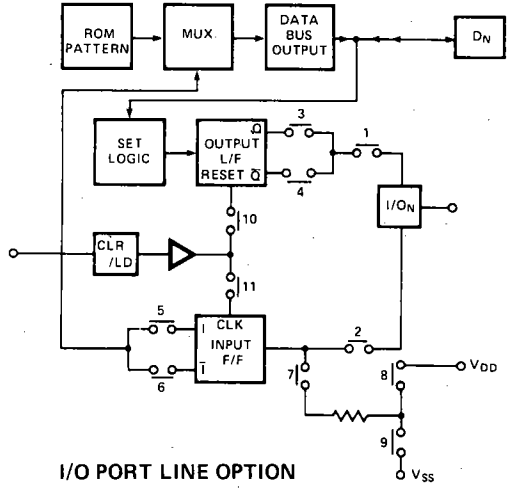
A. CHIP NUMBER _____ (Must be specified).

B. I/O OPTION – Specify the connection numbers for each I/O pin. See table below.

C. 4308 CUSTOM ROM PATTERN – Programming information should be sent in the form of computer punched cards or punched paper tape. In either case, a printout of the truth table must accompany the order. Based on the particular customer pattern, the characters should be written as a "P" for a high level output = V_{SS} (negative logic "0") or an "N" for a low level output = V_{DD} (negative logic "1").

Note that: NOP = BPPPP PPPPF = 0000 0000

PIN		OPTION										
I/O 0_0	27	1	2	3	4	5	6	7	8	9	10	11
I/O 0_1	26	1	2	3	4	5	6	7	8	9	10	11
I/O 0_2	25	1	2	3	4	5	6	7	8	9	10	11
I/O 0_3	24	1	2	3	4	5	6	7	8	9	10	11
I/O 1_0	5	1	2	3	4	5	6	7	8	9	10	11
I/O 1_1	4	1	2	3	4	5	6	7	8	9	10	11
I/O 1_2	3	1	2	3	4	5	6	7	8	9	10	11
I/O 1_3	2	1	2	3	4	5	6	7	8	9	10	11
I/O 2_0	17	1	2	3	4	5	6	7	8	9	10	11
I/O 2_1	16	1	2	3	4	5	6	7	8	9	10	11
I/O 2_2	15	1	2	3	4	5	6	7	8	9	10	11
I/O 2_3	14	1	2	3	4	5	6	7	8	9	10	11
I/O 3_0	21	1	2	3	4	5	6	7	8	9	10	11
I/O 3_1	20	1	2	3	4	5	6	7	8	9	10	11
I/O 3_2	19	1	2	3	4	5	6	7	8	9	10	11
I/O 3_3	18	1	2	3	4	5	6	7	8	9	10	11



I/O PORT LINE OPTION

NOTE: Options 10 and 11 cannot both be specified.